

**DESIGNING WITH L4973, 3.5A HIGH EFFICIENCY  
DC-DC CONVERTER**

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**INTRODUCTION**

The L4973 family is a 3.5A monolithic dc-dc converter, step- down topology, operating in continuous mode. It is realized in BCD60 II technology, and it's available in two plastic packages, POWER-DIP18(12+3+3) and SO20L (12+4+4).

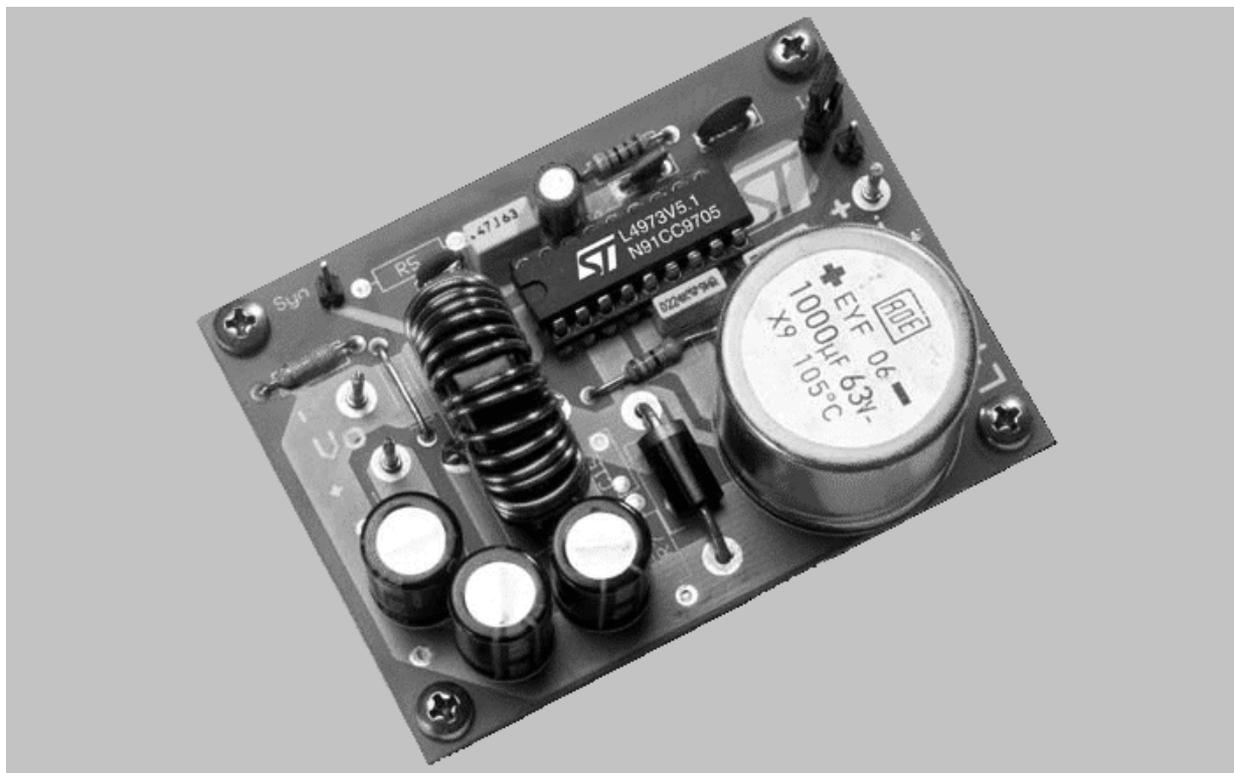
Two versions are available, one fixing the output voltage, without any voltage divider, at 3.3V, and the second at 5.1V.

Both the regulators can control higher output voltage values, by using an external voltage divider.

The operating input supply voltage is ranging from 8V to 55V, while the absolute value, with no load, is 60V.

New internal design solutions and superior technology performance allowed us to develop and produce a device with improved efficiency in all the operating conditions and reduced external component counts.

While internal limiting current and thermal shutdown are today considered standard protections functions mandatory for a safe load supply, oscillator with voltage feedforward will improve line regulation and overall control loop. Soft-start does not allow output overvoltages at turn-on, and synchronization function can reduce EMI problems in multioutputs power supplies. Inhibit, introduced for power management, in equipments having stand-by features, when active( high), reduces the device power consumption, signal plus power stages, at few tens of  $\mu$ A.

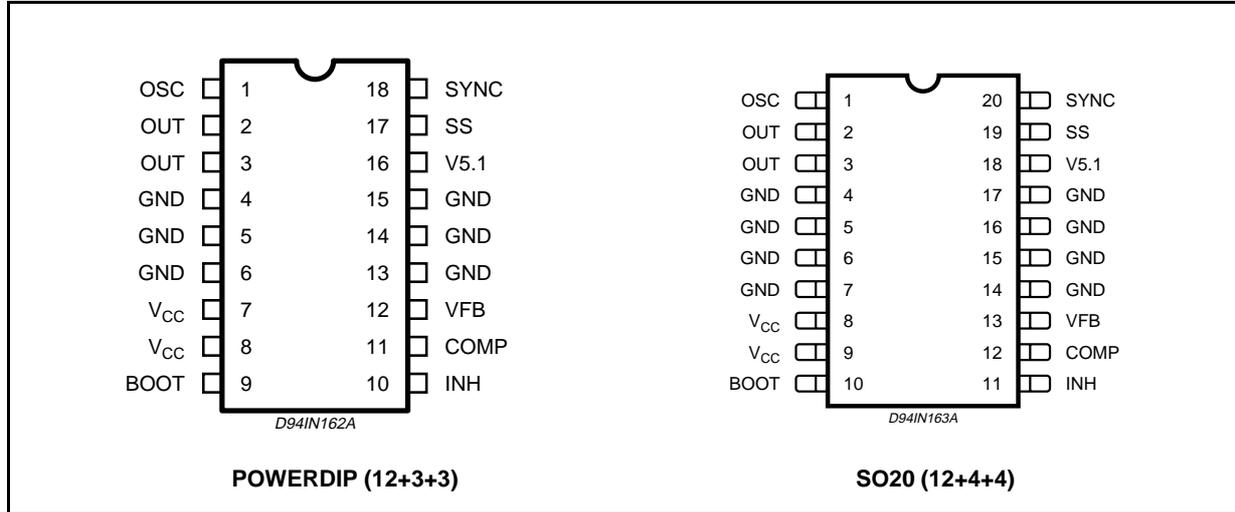


# AN938 APPLICATION NOTE

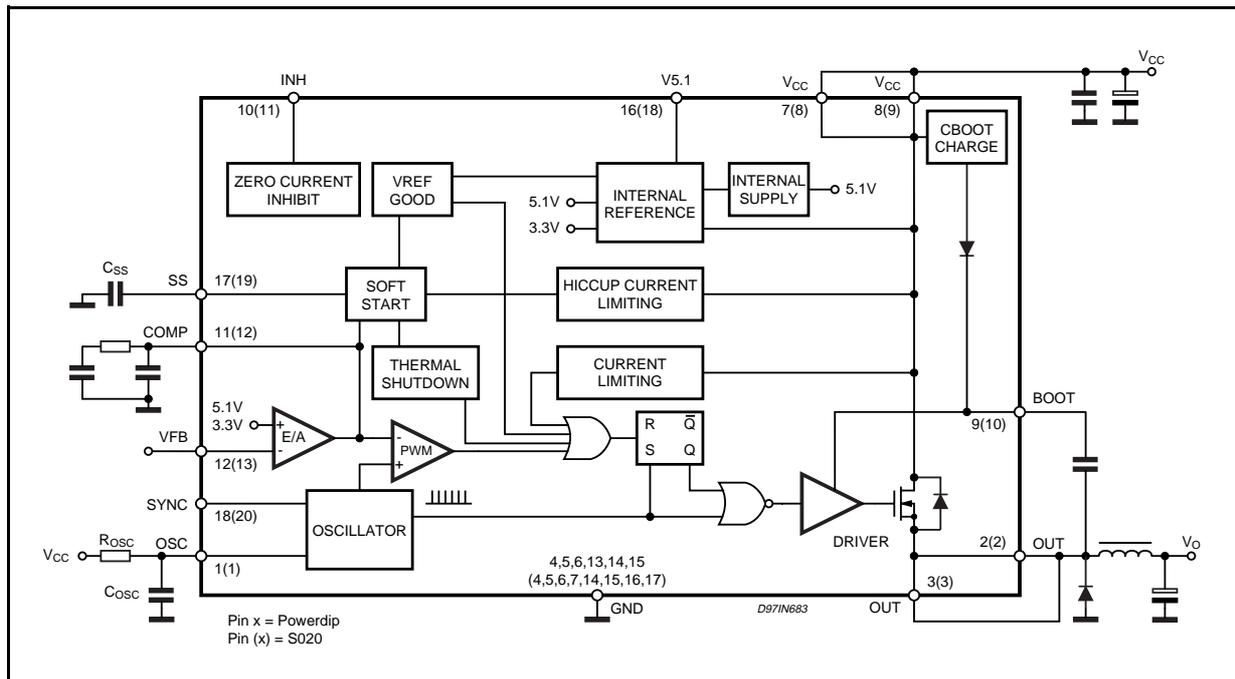
## DEVICE DESCRIPTION

For a better understanding of the device and its working principle, a short description of the main building blocks is given here below, with packaging options and complete block diagram.

**Figure 1. Two packaging options, with the pin function assignments.**



**Figure 2. Device block diagram.**



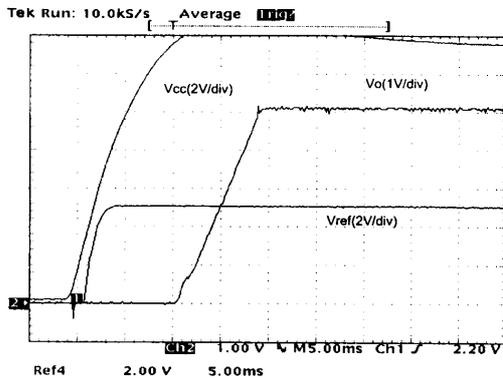
### POWER SUPPLY, UVLO and VOLTAGE REFERENCE.

The device is provided with an internal stabilised power supply (of about 12V typ.) that powers the analog and digital control blocks and the bootstrap section.

Moreover, a safe turn-on sequence is guaranteed by an internal UVLO.

When the supply voltage is reaching about 3.8V, the band-gap goes into regulation, while the internal 5.1V reference starts to increase from zero to its nominal value.

Figure 3.



At 6.5V of Vcc, the device initiates to charge the soft-start capacitor and the power stage generates the first pwm pulses.

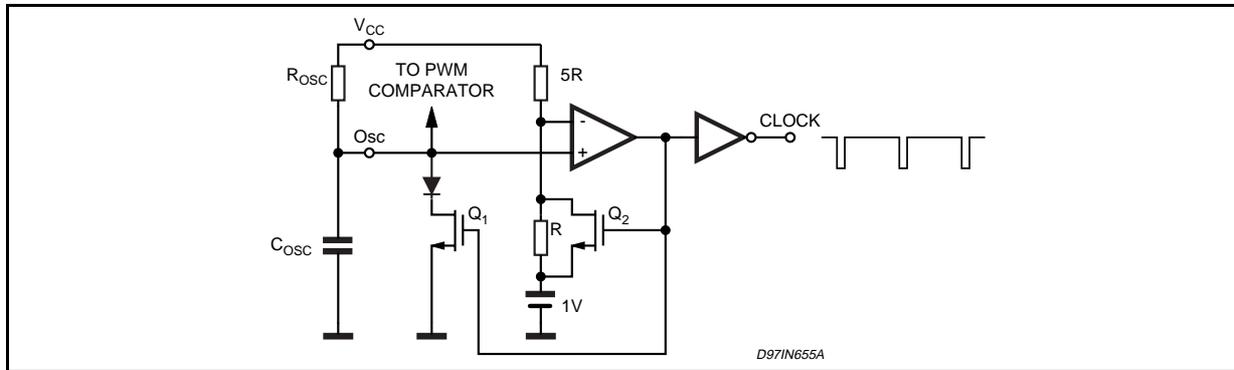
The output voltage increases with a slope controlled by the soft-start time.

Fig. 3 shows the turn-on sequence of the mentioned signals.

From the 12V preregulator, a stable 5.1V +/- 2% reference voltage, externally available, is generated, with a 10mA of current capability.

This reference is available on both types, while the feedback reference is 5.1V for the L4973V5.1 and 3.3V for the L4973V3.3.

Figure 4. Oscillator Internal Circuit.



Oscillator, sync and voltage feedforward

One pin is necessary to implement the oscillator function, with inherent voltage feedforward; a second pin is dedicated to in/out synchronization.

A resistor  $R_{osc}$  and a capacitor  $C_{osc}$  connected as shown in fig. 4, allow the setting of the desired switching frequency in agreement with the below formula:

$$F_{sw} = \frac{1}{R_{Oasc} \cdot C_{Osc} \ln\left(\frac{6}{5}\right) + 100 \cdot C_{Osc}}$$

Where  $F_{sw}$  is in kHz,  $R_{osc}$  in  $K\Omega$  and  $C_{osc}$  in nF.

The oscillator capacitor,  $C_{osc}$ , is discharged by an internal mos transistor of  $100\Omega$  of  $R_{dson}$  ( $Q_1$ ) and during this period the internal threshold is setted at 1V by a second mos,  $Q_2$ . When the oscillator voltage capacitor reaches the 1V threshold the output comparator turn-off the mos  $Q_1$  and turn-on the mos  $Q_2$ , restarting the  $C_{osc}$  charging. The oscillator block, shown in fig. 4, generates a sawtooth wave signal that sets the switching frequency of the system.

This signal, compared with the output of the error amplifier, generates the PWM signal that will modulate the conduction time of the power output stage.

The way the oscillator has been integrated, does not require additional external components to benefit of the voltage feedforward function.

Figure 5. Device switching frequency vs  $R_{osc}$  and  $C_{osc}$ .

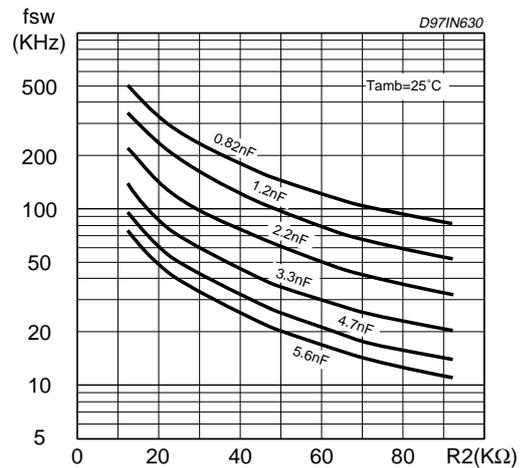
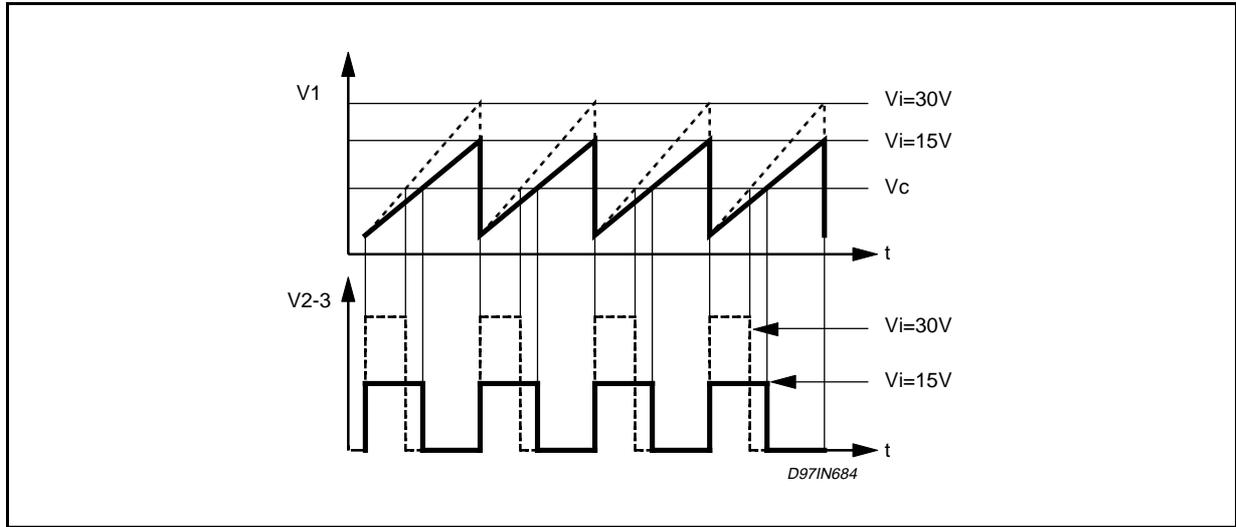


Figure 6. Voltage Feedforward Function.



The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feedforward is operative from 8V to 55V of input supply.

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the  $\Delta V/\Delta t$  of the sawtooth is directly proportional to the supply voltage. As  $V_{CC}$  increases, the  $T_{on}$  time of the power transistor decreases in such a way to provide to the choke, and finally also the load, the product Volt. sec constant.

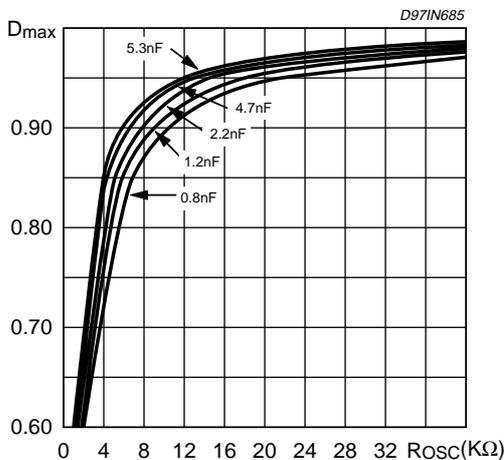
Fig 6 show how the ducty cycle varies as a result of the change on the  $\Delta V/\Delta t$  of the sawtooth with the  $V_{CC}$ .

The output of the error amplifier doesn't change to maintain the output voltage constant and in regulation.

With this function on board, the output response time is greatly reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greatly reduced too.

In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tents of Volt, for both off-line and dc-dc converters using mains transformers.

Figure 7. Maximum Duty Cycle vs.  $R_{osc}$  and  $C_{osc}$  as parameter.



The charge and discharge time is approximable to:

$$T_{ch} = R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right)$$

$$T_{dis} = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of  $T_{ch}$ ,  $T_{dis}$  and an internal delay and is represented by the equation:

$$D_{max} = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^{-9}}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

and is represented in figure 7:

**Current protection**

The L4973 has two current limiting, pulse by pulse and hiccup mode. Increasing the output current till the pulse by pulse limiting current threshold (I<sub>th1</sub> typ. value of 4.5A) the controller reduces the on time, maintaining the peak current at the value:

$$I_p = I_{th1} + (V_{CC} - V_o - R_{on} \cdot I_{th1}) \cdot \frac{t_d}{L_o}$$

where t<sub>d</sub> is the internal propagation delay of the current protection loop (typical 300ns).

If the operating conditions define a min on time lower than t<sub>d</sub>, the current increases to the following value:

$$I_{max} = \frac{(V_{CC} \cdot t_d \cdot F_{sw} \cdot V_f \cdot (1 - t_d \cdot F_{sw}))}{(R_o + R_{on} \cdot t_d \cdot F_{sw})}$$

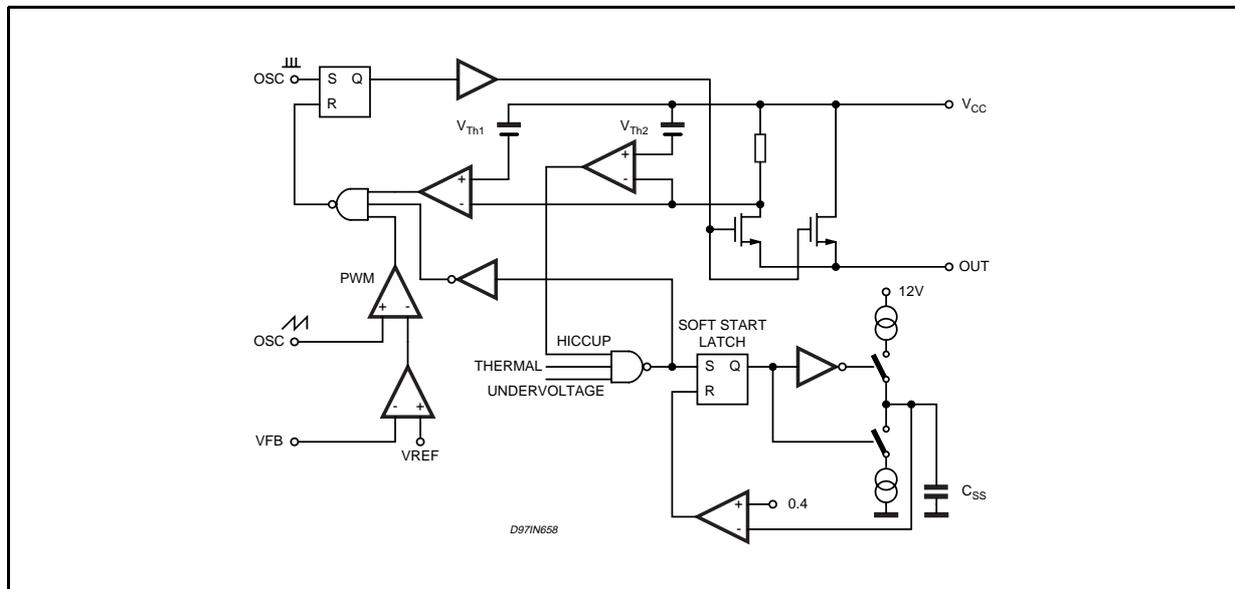
Where R<sub>o</sub> is the load resistance, V<sub>f</sub> is the diode forward voltage and F<sub>sw</sub> is the switching frequency.

The output characteristic is represented in fig 8. At point A the output voltage drops, and the device is going to pulse by pulse limiting current. Getting closer to the output short circuit, the current is shifting to point B, a bit higher because of the ripple current reduction and because hiccup intervention, setted 20% higher than pulse by pulse one.

Once the hiccup limiting current is operating, in output short circuit conditions the delivered average output current is the value at point C.

Fig. 9 shows the internal current limiting circuitry. V<sub>th1</sub> is the pulse by pulse while V<sub>th2</sub> is the hiccup threshold.

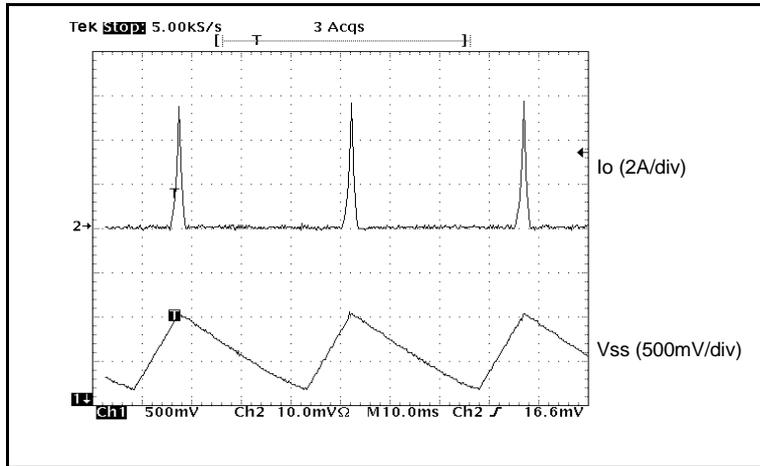
**Figure 9. Internal Current Limiting Schematic Diagram.**



The sense resistor is in series with a small mos realized as a partition of the main DMOS.

The V<sub>th2</sub> comparator (20% higher than V<sub>th1</sub>) Sets the soft start latch, initializing the discharge of the soft start capacitor at constant current (about 22µA).

Figure 10. Output current and soft start voltage.



When reached about 0.4V, the valley comparator Resets the soft start latch, restarting a new soft-start recharging cycle.

Fig. 10 Shows the typical waveforms of the current in the output inductor and the soft start voltage (pin17).

If the short circuit is permanent when the on time reach the internal delay the system recognize that the short circuit is still present and discharge again the soft start capacitor.

The soft start capacitance value must not be too high because the system cannot intervenes before the on time reach the internal delay time. In output short circuit condition the

current increase cycle by cycle because the inductor during the off time cannot recycles all the energy stored during the on time.

It is necessary to ensure that during the soft start slope the current does not reach values that exceeds 7.5A.

The following diagrams of Fig. 11a and Fig. 11b show the maximum allowed soft start capacitor value as a function of the input voltage, inductor value and switching frequency. The soft start capacitance must not be zero. A minimum value is necessary to guarantee, in short circuit condition, the correct functionality of the internal limiting current circuitry.

Example: For a maximum Vcc of 50V, at 100kHz, with an inductor of 140μH, it is possible to use a soft start capacitor lower than 470μF (see fig. 11a). With such a value, the soft start time (see fig. 13) of about 10ms for an output voltage of 5V

Figure 11a. Maximum soft start capacitance with f<sub>sw</sub> = 100kHz

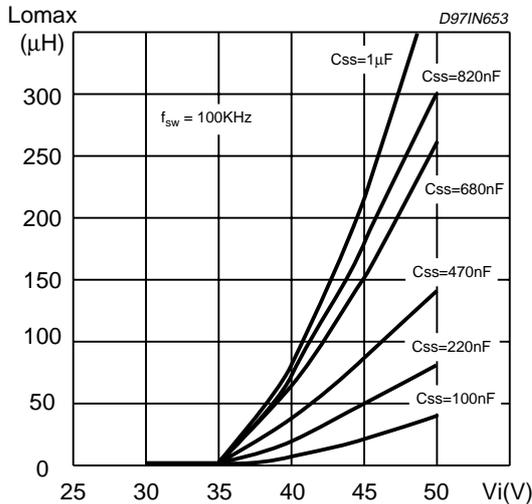
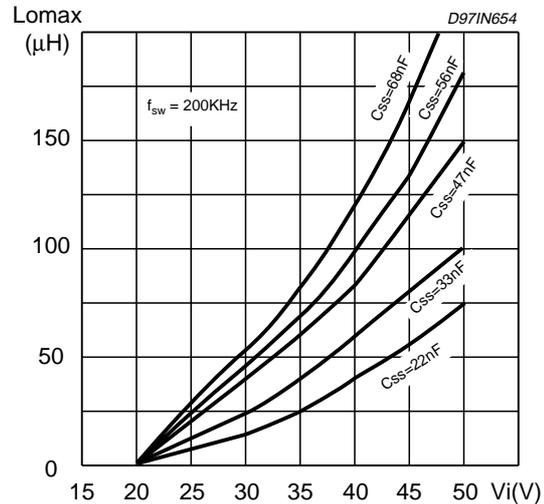


Figure 11b. Maximum soft start capacitance with f<sub>sw</sub> = 200kHz



**Soft Start**

The soft start function is requested to realize a correct start up of the system without overstressing the power stage, avoiding the intervention of the current limiting, and having an output voltage rising smoothly without output overshoots.

The Soft start circuit is shown in fig 12.





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If the feedback is disconnected, open loop, and the impedance at pin 12 is higher than 3.5MΩ, the voltage at this pin goes higher than the internal reference voltage located on the non-inverting error amplifier input, and turns-off the power device.

### Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke. In light load conditions, this topology tends to operate in burst mode, with random repetition rate of the bursts.

This device, in particular, is capable to regulate the output voltage till the load is going to 1mA only. Lower than 1mA load, up to 500μA, the output regulation is guaranteed up to 8% above the nominal value.

There are two circuits providing for the control :

1- an internal comparator located on the bootstrap section is sensing the bootstrap voltage; when lower than 5V, the internal power device is switched on for about 300nsec, allowing the recharge of the bootstrap capacitor.

2- a comparator located on the E/A area, with an input connected to pin12 and the second to a threshold 8% higher than nominal output, turns off the internal power device when Vo is reaching that value.

When the load is lower than 500μA, that is also the current consumption of the bootstrap section, the output voltage starts to increase, approaching the supply voltage.

### Output Overvoltage Protection (OVP)

The output overvoltage protection, OVP, is realized by using an internal comparator, which input is connected to pin 12, the feedback, that turns-off the power stage when the OVP threshold is reached.

This threshold is typically 8% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage, the OVP intervention will be set at:

$$V_{OVP} = 1.08 \cdot V_{FB} \cdot (R_a + R_b)/R_b$$

where Ra is the resistor connected to the output.

### Power Stage

The power stage is realized by a N-channel D-mos transistor with a Vdss in excess of 60V and typ rdson of 150mΩ (measured at the device pins).

Minimising the Rdson, means also minimise the conduction losses.

But also the switching losses have to be taken into consideration. mainly for the two following reasons:

- a- they are affecting the system efficiency and the device power dissipation
- b- because they generate EMI.

### TURN - ON

At turn-on of the power element, or better, the rise time of the current(di/dt) at turn-on is the most critical parameter to compromise.

At a first approach, it looks that faster is the rise time and lower are the turn-on losses.

It's not completely true.

There is a limit, and it's introduced by the recovery time of the recirculation diode.

Above this limit, about 100A/usec, only disadvantages are obtained:

- 1- turn-on overcurrent is decreasing efficiency and system reliability
- 2- big EMI increase.

The L4973 has been developed with a special focus on this dynamic area.

An innovative and proprietary gate driver, with two different timings, has been introduced. When the diode reverse voltage is reaching about 3V, the gate is sourced with low current (see fig. 15) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise. After this threshold, the gate drive current is quickly increased, producing a fast rise time to reach a high efficiency.

TURN - OFF

The turn-off behavior, is shown at Fig. 15.

Fig. 16 shows the details of the internal power stage and driver, where at Q2 is demanded the turn-off of the power swith, S.

Figure 15. Turn on and Turn off (pin 2, 3)

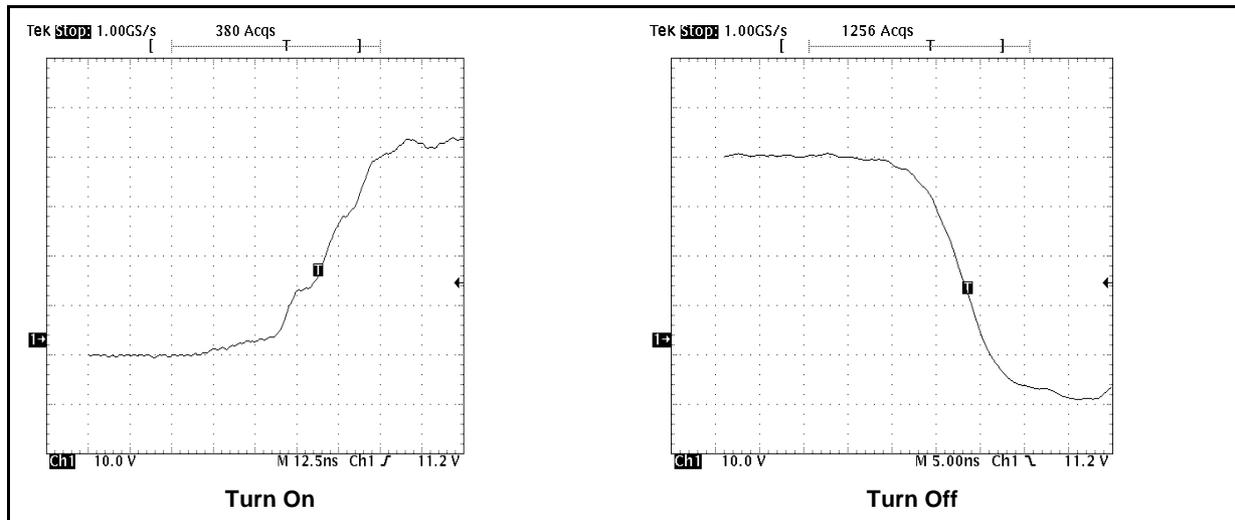
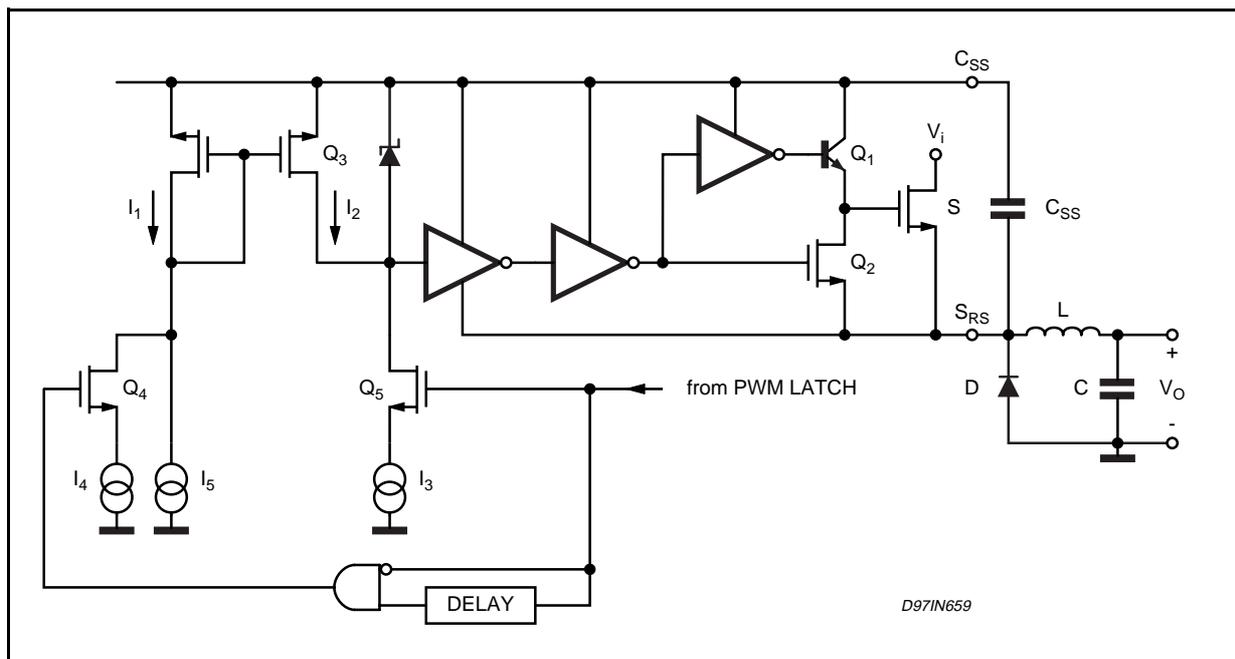


Figure 16. Power stage internal circuit



**Synchronization Function**

The device is able to synchronise other L4973s, up to 6.

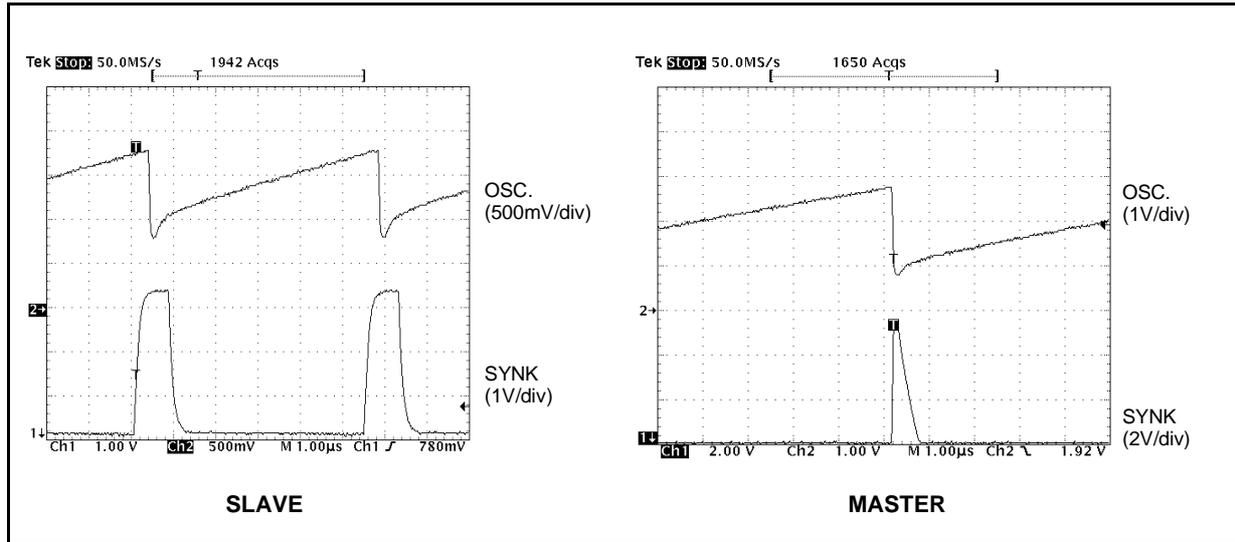
Moreover, this function has been realized to make the device operating as a master or slave.

As a master, it's able to source a current of 3mA min at 4.5V min.

As a slave, it requires a maximum current of 0.45mA and a min pulse width of about 350ns.

Fig. 17 shows the typical synchronization waveforms when the device is used as slave and as master.

**Figure 17. Sync and Oscillator waveforms as slave and as master.**



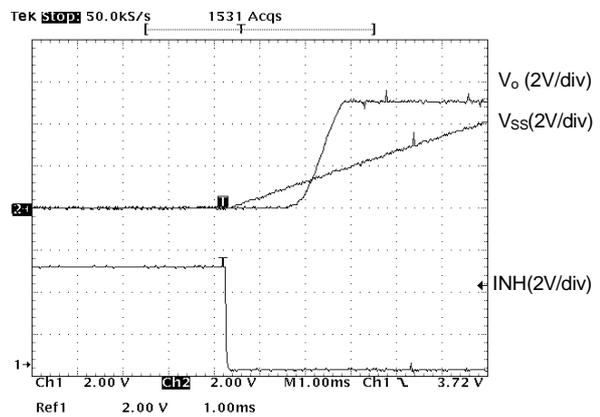
**Inhibit Function**

The Inhibit pin is active high and when left open, is forced to Vcc by an internal current generator and the device is disabled.

In disabled state, Vinh = 5V, the device discharge quickly the soft start capacitor, switch off also the reference voltage, limiting the power consumption to a leakage values only (at 24V, about 100µA).

Fig. 18 shows the device behavior when inhibit pin goes low; the soft start capacitor is linearly re-charged, and the output voltage raises till the nominal value.

**Figure 18. Re-start output voltage when Inhibit goes low (C<sub>ss</sub> = 56nF)**



**TYPICAL APPLICATION.**

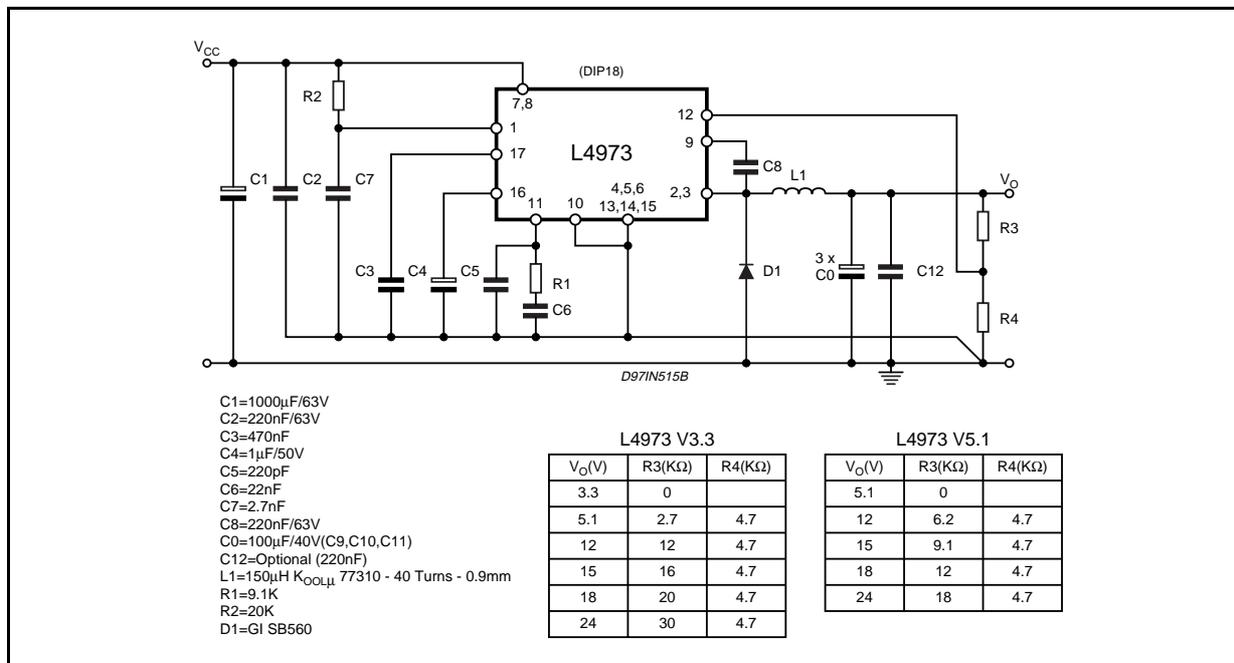
Fig. 19 shows the typical application circuit, where the input supply voltage, V<sub>cc</sub>, can range from 8 to 55V operating, and the output voltage adjustable from 3.3V to 40V.

The selected components, and in particular input and output capacitors, are able to sustain the device voltage ratings, and the corresponding RMS currents.

**Electrical Specification**

Input Voltage Range	8V - 55V
Output Voltage	5.1V ±3% (Line, Load and Thermal)
Output Ripple	50mV
Output Current range	1mA - 3.5A
Max Output Ripple current	15% I <sub>omax</sub>
Current limit	4.5A
Switching frequency	100kHz
Target Efficiency	85% @ 3.5A V <sub>i</sub> = 50V 95% @ 0.5A V <sub>i</sub> = 12V

**Figure 19. Application circuit**



**Input Capacitor**

The input capacitor has to be able to support the max input operating voltage of the device and the max rms input current.

The input current is squared and the quality of these capacitors has to be very high to minimise its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors are also affecting the system efficiency.

The max I<sub>rms</sub> current flowing through the input capacitors is:

$$I_{rms} = I_o \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and I<sub>o</sub> the output dc current.

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This function reaches the maximum value at  $D = 0.5$  and the equivalent rms current is equal to  $I_o/2$ . The following diagram Fig. 20 is the graphical representation of the above equation, with an estimated efficiency of 85%, at different output currents.

The maximum and minimum duty cycles are:

$$D_{\max} = \frac{V_o + V_f}{V_{cc\min} + V_f} = 0.66 \quad D_{\min} = \frac{V_o + V_f}{V_{cc\max} + V_f} = 0.1$$

where  $V_f$  is the freewheeling diode forward voltage.

This formula is not taking into account the power mos  $R_{ds(on)}$ , considering negligible the inherent voltage drop, respect input and output voltages.

At full load, 3.5A, and  $D=0.5$ , the rms capacitor current to be sustained is of 1.75A.

The selected 1000 $\mu$ F/63V EYF or EYS, guaranting a life time of 16000 hours at an ambient temperature of 60°C and switching frequency of 100kHz, can support 1.9A RMS current.

### Output voltage selection

The two available devices can regulate directly the output voltage respectively the L4973V3.3 the 3.3V and the L4973V5.1, the 5.1V.

Each of the two devices can regulate an output voltage higher than the nominal value, up to 40V, by adding an external voltage divider as usually.

In case of requested output voltage lower than 3.3V, it is possible to use the L4973V3.3 with the external connections as shown in fig. 21.

$$V_o = V_{fb} - (V_{ref} - V_{fb}) \cdot \frac{R_3}{R_5}$$

and the relative function is plotted in fig 22.

Only two resistors are used, and all the curves do not intercept the 3.3V but have an asintotic trend to this value.

### Inductor Selection

The criteria used in fixing the inductor value has been dictated by the wanted output ripple voltage, 50mV max., performance obtained of course in combination with output capacitors too.

The inductor ripple current, fixed at 10% of  $I_{omax}$ , i.e., 0.35A, requires an inductor value of:

$$L_o = (V_o + V_f) \cdot \frac{(1 - D_{\min})}{\Delta I_L \cdot f_{sw}} = 140\mu H \quad \text{Eq (1)}$$

The chokesatisfying this request has to sustain an  $L \cdot I_{pk}^2$  of 1.776.

A 77310 (125 $\mu$ ) core, with 40T, can do the job. Material is KoolM $\mu$ , from Magnetics.

Figure 20. Input Capacitance rms current vs. duty cycle

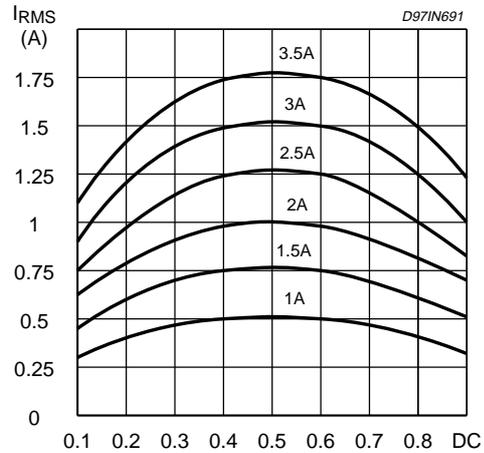


Figure 21. Example of output regulated voltage lower than 3.3V

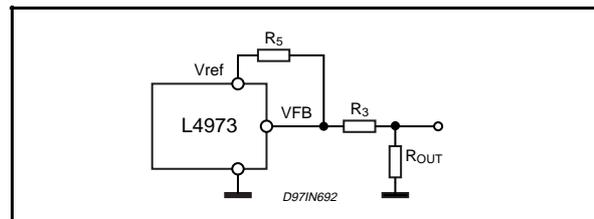
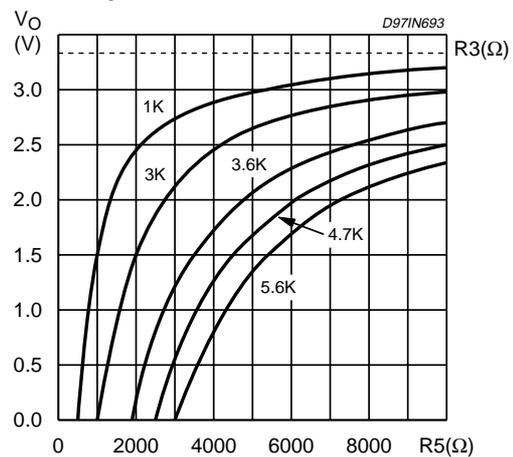


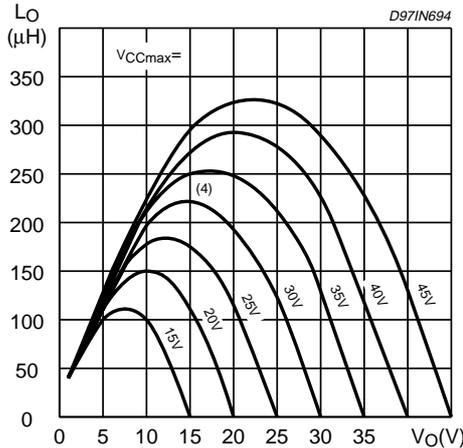
Figure 22. Output voltage vs R5 using R3 as parameter



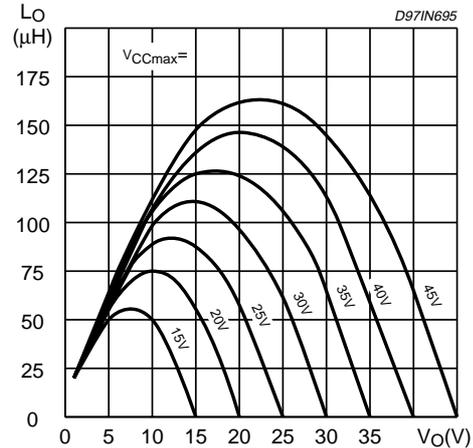
At full load, the magnetizing force is about 25 Oersted; the inductance value is reduced of about 30% and the ripple current increase at 0.5A (14% of Iomax).

It is possible to plot Eq 1 as a function of Vo and Vccmax at 100kHz and 200kHz (see Fig. 23a-b).

**Figure 23a: Ideal inductor value requested for 10% ripple current, as a function of max. input voltage and output**



**Figure 23b: Ideal inductor value requested for 10% ripple current, as a function of max. input voltage and output**



Design example: with a maximum input voltage of 30V, at 100kHz, reference curve is number (4) in Fig. 23a; with an output voltage of 10V, the suggested inductor value is 200uH.

Core losses are also to be considered when evaluation the system efficiency.

They are proportional to the magnetic flux swing, and to evaluate the magnitude of the flux, the following formula can be used:

$$\Delta B = \frac{L \cdot \Delta I_L}{N \cdot A_{le} \cdot 10^{-8}} = 550\text{mGauss}$$

where N is the number of turns and Ale is the core cross section (cm<sup>2</sup>).

The selected core material has the following empirical equation to calculate the core losses:

$$P_l = \Delta B^2 \cdot f_{sw}^{1.5} \cdot V_l = 570\text{mW}$$

Where V<sub>l</sub> is the core volume in cm<sup>3</sup>. The core increasing temperature is:

$$\Delta T = \left( \frac{P_l}{33.8} \right)^{0.833} = 10.5^\circ\text{C}$$

**Output Capacitors**

The output capacitors selection, Co, is mainly driven by the output ripple voltage that has to be guaranteed, in this case 1% max. of Vo.

The output ripple is defined by the ESR of Co and by the maximum ripple current flowing through it, fixed previously at 0.5A max.

The maximum permitted ESR is:

$$\text{ESR} = \Delta V_o / \Delta I_L = 0.051 / 0.5 = 102\text{m}\Omega$$

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The chosen total capacitance is of 3 X 100µF/40V EKR (Frolyt), each of them having an ESR of 230mΩ at 25°C, for a total ripple voltage of 0.76% of Vo, i.e., 40mV.

Co has also to support load transients. An idea of the magnitude of the output voltage drop during load transients is given below:

$$\Delta V_o = \frac{(\Delta I_o)^2 \cdot L_o}{2 \cdot C_o \cdot (V_{inmin} \cdot D_{max} - V_o)} \quad \text{Eq (2)}$$

where  $\Delta I_o$  is the load current change, from 0.5A to 3.5A,  $D_{max}$  is the max. duty cycle, 95%,  $V_o$  nominal is 5.1V, and finally L is 140µH.

Equation 2, normalized at  $V_o$ , is represented in the following diagram, Fig. 24, as a function of the minimum input voltage.

These curves are represented for different output capacitor 3x100µF, 2x220µF, 3x220µF, 2x470µF all EKR, 40V.

### Compensation Network

The complete control loop block diagram is shown in fig. 25

The Error Amplifier basic characteristics are:

$$g_m = 2.5\text{mS}$$

$$R_o = 1.2\text{M}\Omega$$

$$A_{vo} = 60\text{dB}$$

$$I_{source/sink} = 300\mu\text{A}$$

### Error amplifier and compensation blocks

The open loop gain is:

$$A(s) = g_m \cdot \frac{R_o \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

where  $C_{out}$  is the parallel between the output and the external capacitance of the Error Amplifier and  $R_o$  the E/A output impedance.

$R_c$  and  $C_c$  are the compensation values.

### LC Filter

$$A_{o(s)} = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot s + 1}$$

### PWM Gain

$$\frac{V_{cc}}{V_{ct}} = \frac{V_{cc} \cdot 6}{V_{cc} - 1} \approx 6$$

where  $V_{ct}$  is the peak to peak sawtooth oscillator.

Figure 24. Output drop (%) vs minimum input voltage

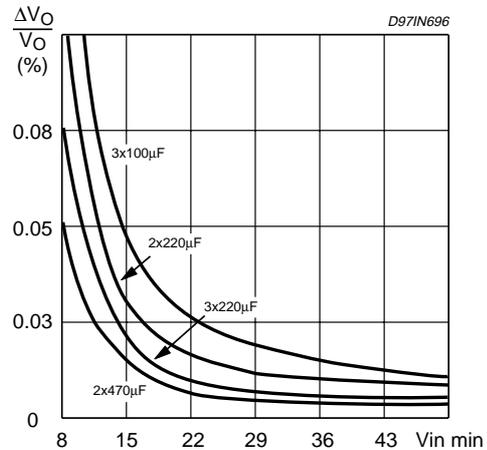


Figure 25. Block diagram compensation loop

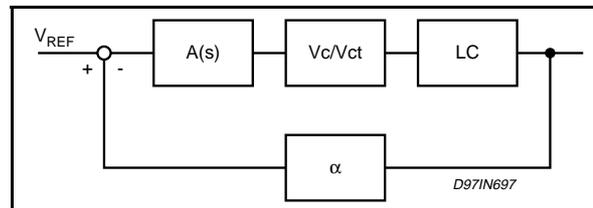


Figure 27.

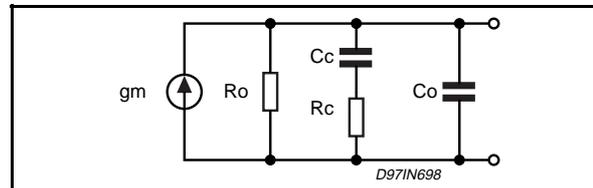
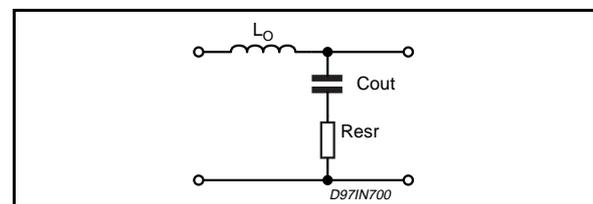


Figure 26.



Output voltage divider

$$\alpha = \frac{R1}{R1 + R2}$$

Poles and zeros value are:

$$F_o = \frac{1}{2 \cdot \pi \cdot R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.077 \cdot 300 \cdot 10^{-6}} = 6.92\text{KHz}$$

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot \sqrt{140 \cdot 10^{-6}} \cdot 300 \cdot 10^{-6}} = 776\text{Hz}$$

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 795\text{Hz}$$

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^6 \cdot 22 \cdot 10^{-9}} = 6.92\text{KHz}$$

$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 80\text{KHz}$$

The compensation is realized choosing the  $F_{ocomp}$  close to the frequency of the double pole introduced by the LC filter.

Using a compensation network with  $R1 = 9.1\text{K}$ ,  $C6 = 22\text{nF}$  and  $C5 = 220\text{pF}$ , the Gain and Phase Bode plots are shown in Fig. 28-29. The cut-off frequency and the phase margin are:

$$F_c = 10\text{KHz} \quad \phi_m = 35^\circ$$

Figure 28. Gain Bode plot open loop

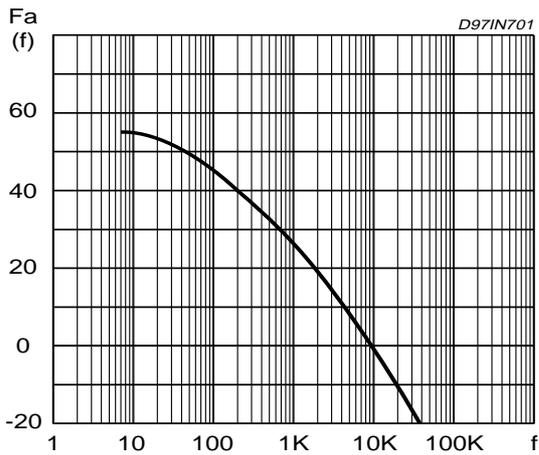
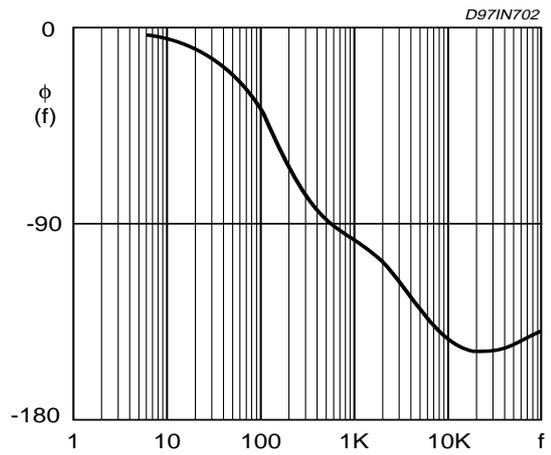


Figure 29. Phase Bode plot open loop

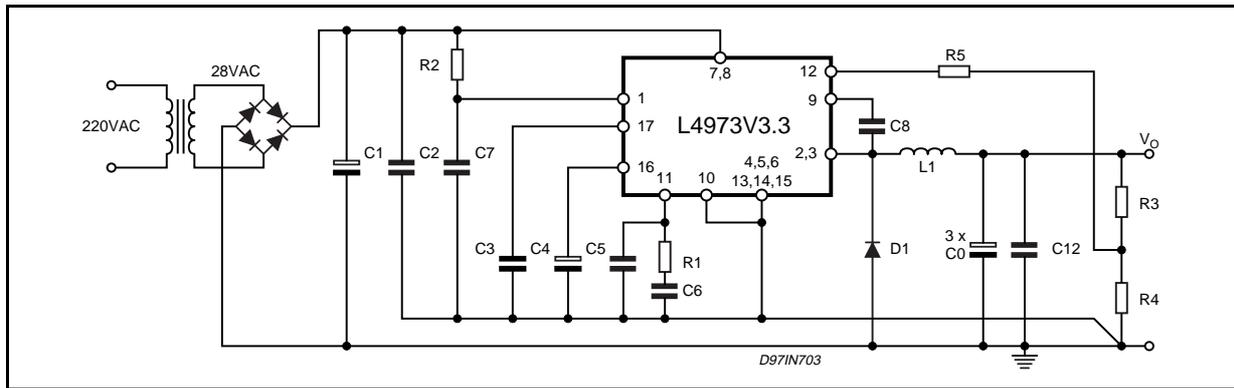


APPLICATION IDEAS

MAINS TRANSFORMER POWER SUPPLY, with output adjustable from 0V to 24V.

Fig A1 shows a power supply including mains transformer, working at 50Hz 220Vac or 60Hz 110Vac, bridge rectifier and filtering capacitor; the output voltage is adjustable from 0 to 24V.

Figure A1. Typical adjustable 0-24V power supply.

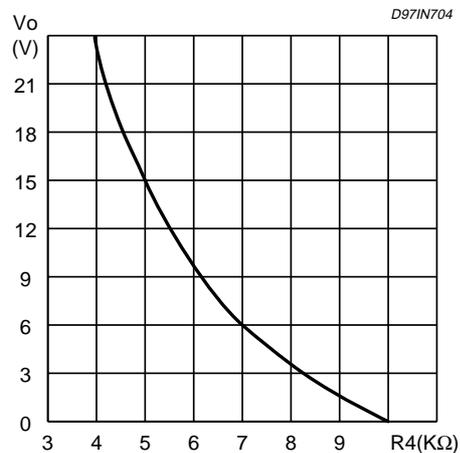


The formula to evaluate the output voltage is:

$$V_o = 3.336 + 3.336 \cdot \left( \frac{R_3}{R_4} + \frac{R_3}{R_4} \right) - 5.1 \cdot \frac{R_3}{R_5}$$

Fig A2 shows the formula plot in which is possible to program the output voltage from 0V to 24V using a 10KΩ potentiometer as R4. R5 is fixed at 4.3KΩ and R3 is 47KΩ.

Figure A2. Output Voltage vs R4



Output capacitors have to be chosen with low ESR to reduce the output ripple voltage and load transients.

Particular care has to be taken for input filter capacitors because they have to support high ripple current at mains frequency plus the high frequency current. Total rms current is typically heavy, and very low ESR is requested for system reliability.

Input caps can affect also the system efficiency.

The transformer could be a single secondary winding with four diodes for rectification or centre tapped with two diodes only, but higher reverse voltage.

Considering a max output power close to 100W, equivalent system efficiency of 93-95%, the mains transformer has to be designed around 200VA.

A low voltage secondary pfc can reduce the VA need close to the delivered Watts, 110W, reducing also the electrolytic capacitors value .

Weight and volume of the complete application are also significantly reduced.

HIGHER INPUT VOLTAGE

Since the max. operating input voltage is 55V, an input line conditioner is requested.

Fixing, for example, the device supply voltage at 50V, the power dissipation of the preregulator is :

$$P_d = I_i \cdot V_{ce} = I_i \cdot (V_i - 50)$$

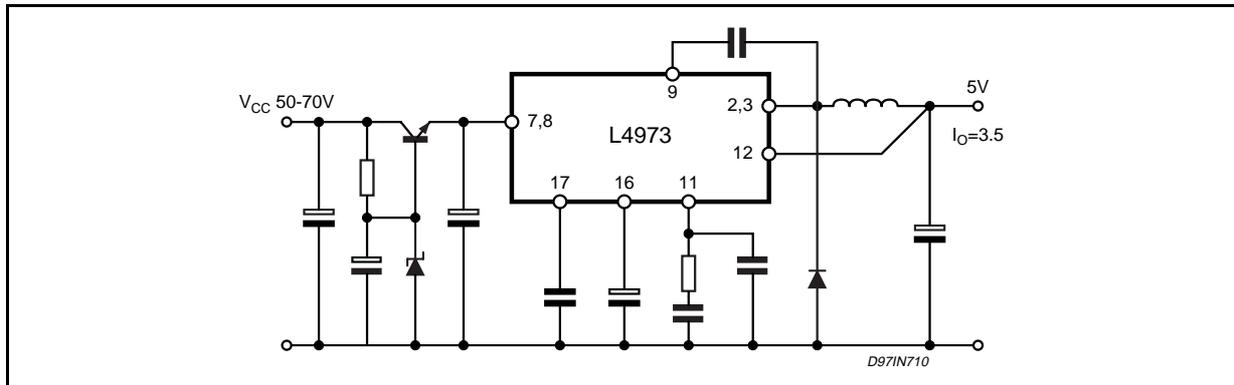
In the buck converter, the average input current is:

$$I_i = I_o \cdot T_{on}/T = I_o \cdot V_o/V_i$$

-)  $V_o = 5.1V$   $I_o = 3.5A$   $P_o = 17.85W$   $I_i = 0.357A$   $P_d = 3.57W$  ( $V_i = 60V$ )

-)  $V_o = 12V$   $I_o = 3.5A$   $P_o = 42W$   $I_i = 0.84A$   $P_d = 8.4W$  ( $V_i = 60V$ )

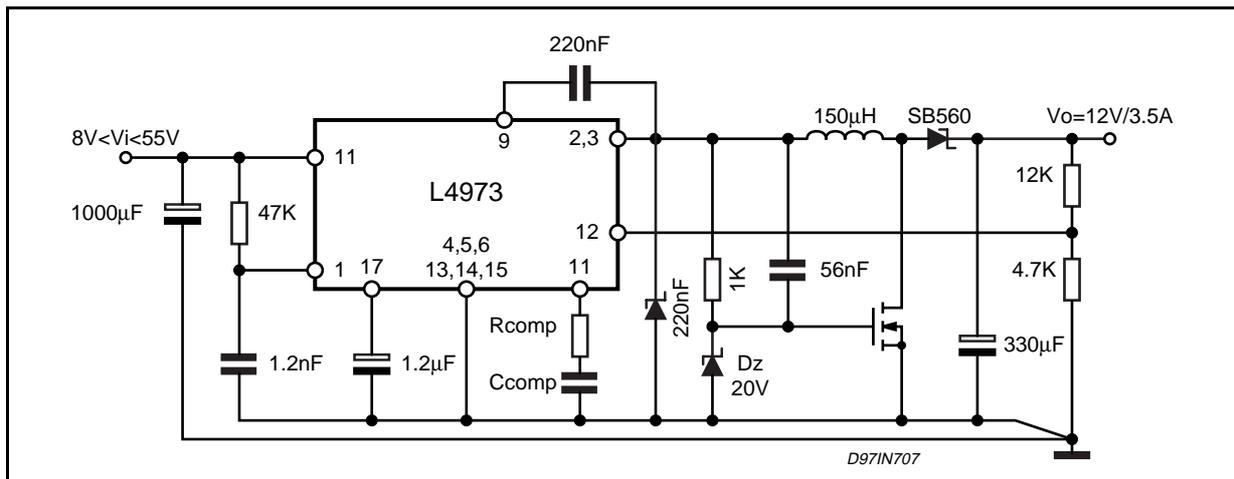
Figure A3. Design example for 70V input supply.



### BUCK-BOOST CONVERTER

This topology is useful to stabilise an output voltage higher, equal or lower than the input supply. Fig A4 shows the schematic diagram of a converter designed for 12V, 3.5A output, with an input supply ranging from 8V to 24V.

Figure A4. Up Down Converter



The 20V zener connected to gate-source of the power mos is from protection purposes when the supply voltage is higher than 20V.

Such a circuit, asymmetrical half bridge, is fully protected versus output short circuit, by turning-off the

## AN938 APPLICATION NOTE

on-board floating mos.

### CURRENT GENERATOR

Sometime the applications specs requires to generate constant current, fixed or adjustable, for chemical processes, lamp powering, battery chargers for lead acids, ni-cd and ni-me-hyd batteries.

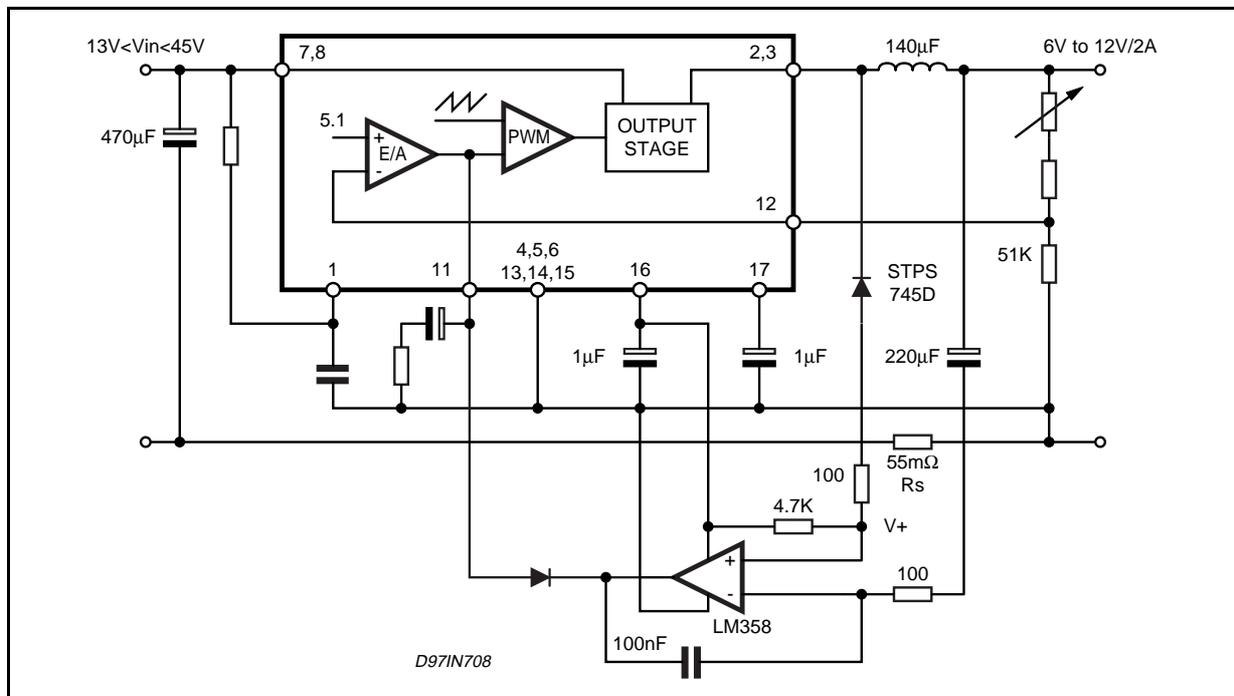
Here, one suggestion will be given for obtaining an accurate constant current generator.

The schematic of Fig A5 propose a simple solution for constant or variable current generator, with good accuracy of the current, using a simple op/amp supplied by the 5.1V available reference voltage. The threshold current is fixed by the voltage divider connected to the n.i. input op/amp, at about 100mV. This is also the max voltage dropping on the current sense resistor  $R_s$ . Adjusting the 4.7KOhm, the threshold can be easily changed.

The formula to fix the output current is :

$$I_o = \frac{5.1 \cdot R_2}{(R_1 + R_2) \cdot R_s}$$

**Figure A5. Constant current generator, up to 3.5A.**



### FROM POSITIVE INPUT TO NEGATIVE OUTPUT

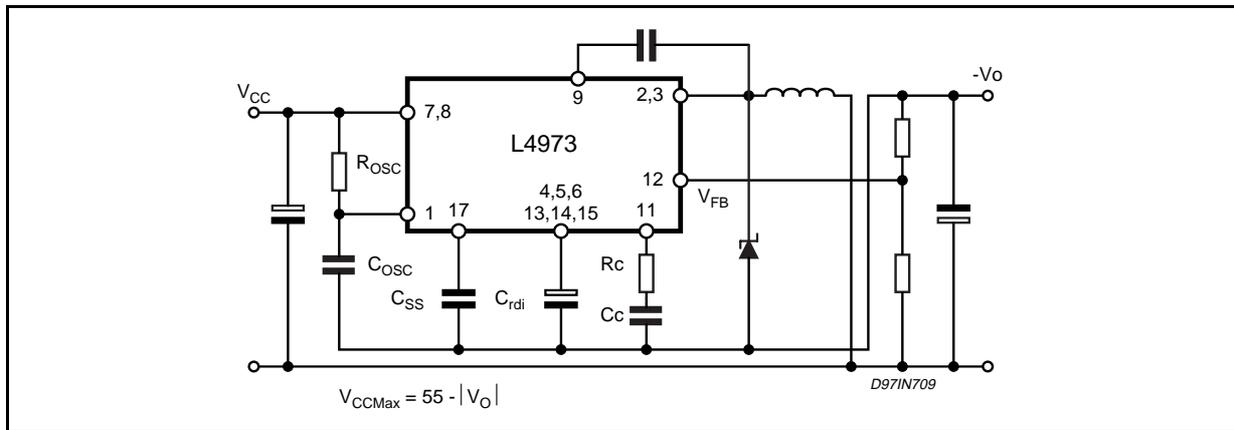
Fig. A6 shows how to obtain a -12V, couple of Amps, when only positive supply available.

This negative output has to show good precision, stability and regulation, and it must be output short circuit protected.

With the suggested application schematic, one the aim is to satisfy the performance listed above, and to contributing to the simplification of the power transformer, mains or high frequency.

Just to remember not to exceed the absolute maximum voltage rating of the device of 55V operating. In this case the total voltage applied to the device is the addition of the max. positive input voltage with the min. negative output voltage.

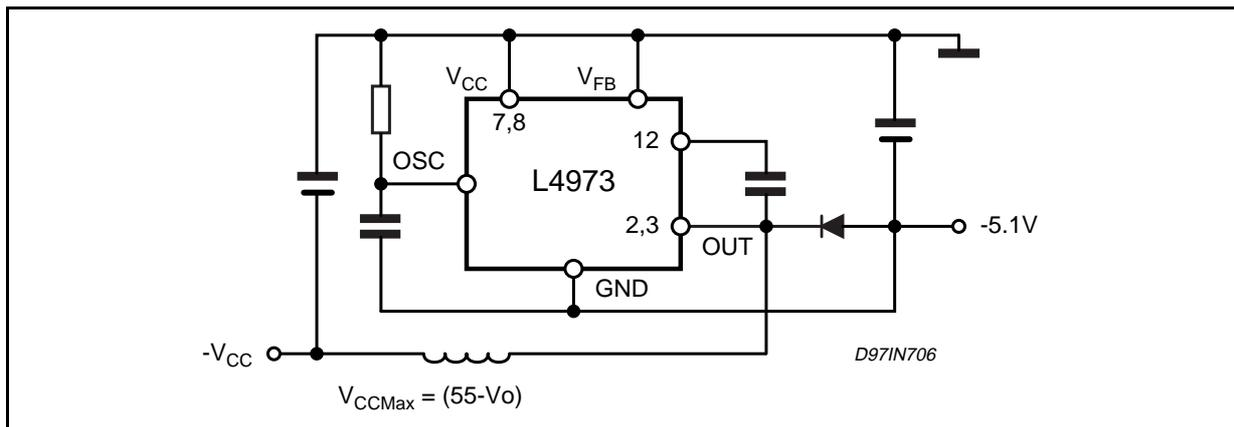
Figure A6. Negative Output Voltage.



**NEGATIVE BOOST CONVERTER**

Fig. A7 shows how to stabilise a negative output voltage higher than negative input voltage.

Figure A7. Negative boost converter.



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